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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/758,040	01/16/2004	Sung-kyu Choi	Q78894	6125

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EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2111	

MAIL DATE	DELIVERY MODE
05/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 10/758,040	**Applicant(s)** CHOI, SUNG-KYU	
	Examiner Christopher E. Lee	**Art Unit** 2111	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 17 May 2007 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires 4 months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☒ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: 1-10.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☒ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

Christopher E. Lee
Primary Patent Examiner
Art Unit: 2111

Continuation of 11. does NOT place the application in condition for allowance because:
In response to the Applicant's argument with respect to the Preliminary Matters regarding to Declaration under 37 CFR §1.131 for overcoming the reference Barrenscheen of the record in the Response pages 2-3, the Declaration under 37 CFR §1.131 has not been entered because the Applicant fails to provide a showing of good and sufficient reasons why the affidavit or other evidences is necessary and was not earlier presented, under 37 CFR §1.116(e).
Therefore, the request for consideration of the Declaration under 37 CFR §1.131 has not been considered because the Declaration under 37 CFR §1.131 has not been entered.

In response to the Applicant's argument with respect to "... Applicant respectfully submits that claim 1 would not have been rendered obviousness by Bourke and Barrenscheen. There is simply no disclosure in Barrenscheen that the Bus interface, BI1 acts as or performs the functions of a multiplexer." in the Response page 4, line 2 through page 5, line 3, this argument had been properly responded in the Final Office Action mailed on 18th of January 2007 (hereinafter the Final Office Action), and the Examiner respectfully disagrees.
Basically, the Applicant recites the claimed subject matter "multiplexer" with the limitation "wherein the multiplexer receives first data from the processor and transfers the received first data to a first memory through a synchronous data bus synchronized with the processor, or receives second data from the first memory through the synchronous data bus and transfers the received second data to the processor" (See Claim 1, lines 11-14), and further, the Applicant specifies that the claimed subject matter "multiplexer" is no more specific component than an interfacing component among processor, buffer, synchronous data bus, and asynchronous data bus, which is disclosed in the specification, page 20, paragraphs [54]-[55], and Figs. 3-4.
Therefore, in contrary to the Applicant's statement, i.e., bus interface BI1 does not act as or perform the functions of a multiplexer in Barrenscheen, Barrenscheen is clearly suggesting the claimed subject matter "multiplexer (i.e., Bus Interface BI1 in Fig. 4)" receiving first data from a processor (e.g., Module BU11 in Figs. 2A-B; See Barrenscheen, paragraph [0029]) and transfers the received first data to a first memory (e.g., Module BU12 in Figs. 2A-B; See Barrenscheen, paragraph [0029]) through a synchronous data bus (i.e., BUS1 in Figs. 2A-B) synchronized with the processor (See Barrenscheen, paragraph [0035], lines 11-12; for example, DMA data writing operation from said Module BU11 to said Module BU12 in Fig. 2A), or receives second data from the first memory through the synchronous data bus and transfers the received second data to the processor (See Barrenscheen, paragraph [0035], lines 11-12; for example, DMA data reading operation from said Module BU12 to said Module BU11 in Fig. 2A). In other words, the recited claiming language "multiplexer," and its function in the exemplary claim 1 are interpreted as the bus interface BI1 performs the functions of and is described as the claimed subject matter "multiplexer" in Barrenscheen.
Thus, the Applicant's argument on this point is not persuasive.

In response to the Applicant's argument with respect to "The Examiner also maintains that Barrenseheen discloses that BUS1 is synchronized with the processor, and cites paragraph [0035] of Barrenscheen as allegedly disclosing this feature of claim 1. However, paragraph [0035] merely discloses that when the data transmission device (DTU) is used as a DMA controller, it can transmit data between devices connected to the same bus or between devices connected between different buses autonomously. There is simply no disclosure in Barrenscheen that the BUSI is synchronized with a processor." in the Response page 5, lines 4-9, this argument had been properly responded in the Final Office Action, and the Examiner respectfully disagrees.
Basically, one of the ordinary skill in the art of digital computer system could understand that the statement "the DTU used as a DMA" in Barrenscheen, paragraph [0035], clearly anticipates the claimed limitation "a synchronous data bus synchronized with the processor," such that BUS1 (i.e., synchronous data bus) is synchronized with Module BU11 (i.e., processor) because it was well known in the art of digital computer system as a common knowledge at the time the invention was made. Furthermore, the Examiner doubts how the DTU can transmit data from one of the devices (i.e., Module BU11) to another device (i.e., Module BU12), which are connected to the BUS1, when the DTU is used as a DMA controller if the BUS1 is not synchronized with the Module BU11.
Thus, the Applicant's argument on this point is not persuasive.

In response to the Applicant's argument with respect to "First, there is simply no teaching or suggestion in Masayuki of synchronous and asynchronous buses. Masayuki teaches a method of preventing delays on an image data bus and improving signal processing efficiency by controlling/managing the read-out and write-in process of storage means connected to the image data bus. Nowhere does Masayuki disclose synchronizing a data bus with a processor. The fact that Masayuki teaches a signal processing unit which prevents delay of image data does not necessarily mean that this "inherently" teaches that the image data bus is synchronized with the CPU as alleged by the Examiner." in the Response page 6, lines 12-18, this argument had been properly responded in the Final Office Action, and the Examiner respectfully disagrees.
Masayuki discloses a signal processing unit (See Title), wherein a synchronous data bus (i.e., CPU bus 34 of Fig. 2) synchronized with a processor (i.e., CPU 41 of Fig. 2) and an asynchronous data bus (i.e., image data bus 33 of Fig. 2) not synchronized with the processor (i.e., said image data bus being synchronized by sync generator 26 of Fig. 1, and said CPU being communicated via several interfaces in Fig. 1).
Even though the Applicant argues that Masayuki does not disclose any particular terms related to 'synchronous' and 'asynchronous', Masayuki clearly suggests CPU (i.e., processor) and CPU bus (i.e., synchronized bus with said CPU), and further, image data bus (i.e., asynchronous data bus) being synchronized by Sync Generator in the Signal Processor, not being synchronized with said CPU (i.e., processor).
Furthermore, in contrary to the Applicant's assertion, i.e., the Examiner alleges that a signal processing unit which prevents delay of image data inherently teaches that the image data bus is synchronized with the CPU, the Examiner has never alleged the Applicant's assertion.
Thus, the Applicant's argument on this point is not persuasive.

In response to the Applicant's argument with respect to "Second, the comments in the Office Action regarding inherency are not understood; the principle of inherency is applicable only with respect to 35 U.S.C. § 102 rejections. Inherency and obviousness are

distinct concepts. A retrospective view of inherency is not a substitute for some teaching or suggestion that supports the selection and use of the elements in the particular claimed combination. In deciding that a novel combination would have been obvious, there must be a supporting leaching in the prior art; for that which may be inherent is not necessarily known, and obviousness cannot be predicated on what is unknown. See In re Newell U.S.P.Q.2d 1248, 1250 (Fed. Cir, 1989)." in the Response page 7, lines 1-8, the Examiner believes that the Applicant does not understand the claim rejection.

First of all, the Office Action has never depending on the retrospective view of inherency for any claim rejection under 35 U.S.C. §102 and/or §103 at all.

Secondly, the comment "inherency" in the argument's response of the Final Office Action is not the retrospective view of inherency because the single reference Masayuki clearly discloses that two busses are separately operating in order to prevent delay of image data bus (See Masayuki, paragraphs [0007]-[0008]). In order words, the fact of the claimed subject matters "synchronous bus" and "asynchronous bus" is suggested by the single reference Masayuki in contrary to the Applicant's asserted "retrospective view of inherency" without any fact from the prior art.

At third, in contrary to the Applicant's allegation, i.e., the principle of inherency is applicable only with respect to 35 U.S.C. § 102 rejections, the inherent disclosure of a prior art may be relied upon in the rejection of claims under 35 U.S.C. §102 or §103. See MPEP 2112 [R-3] Requirements of Rejection Based on Inherency; Burden of Proof.

Thus, the Applicant's argument on this point is not persuasive.